Microtechnology in the Development of Three-Dimensional Circuits

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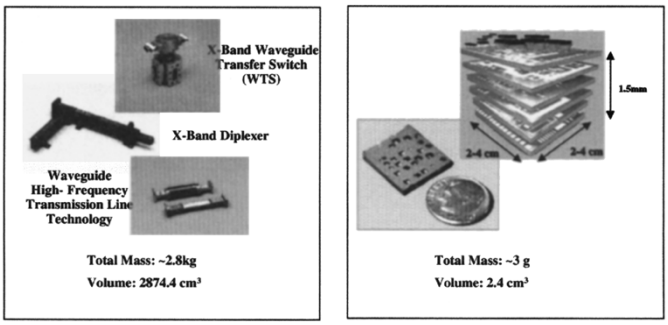
(Invited Paper)

***Abstract*— With today's cost-conscience industry, low-cost, high-performance, and high-profit microwave-circuit technologies are essential. To increase density and reduce size and cost, the integration of analog and digital circuits on one single chip is considered the most viable solution. In reducing the size of the overall system, high-density integration (HDI) and packaging have become critical components in circuit design. This paper reviews and evaluates state-of-the-art planar transmission lines and vertical interconnects for use in high-density multilayer circuits for silicon- and SiGe-based monolithic high-frequency circuits. Packaging issues associated with parasitics will be discussed and examples of multilayer three-dimensional systems utilizing micromachining will be presented.**

***Index Terms*— Coplanar waveguide, micromachining, microstrip, MMIC.**

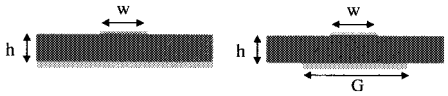
I. Introduction

OVER THE PAST 40 years, the progress of technology and invention of the transistor have made it apparent that very small transmission lines compatible with planar solid-state technology are needed to effectively couple power of microscopic devices, such as integrated circuits, into macroscopic systems, such as satellite communication systems. It is solid-state device technology that has driven the development of planar monolithic microwave integrated circuits (MMIC's) that dominate today's communications systems. This technology has allowed for the design of small RF circuits that combine many functions on a single circuit while providing high performance and low cost. Spacecraft communications systems have benefited tremendously from these advances as applied to microelectronics and very large-scale integration (VLSI), and have experienced steady decreases in both cost and communication system mass. During the past two decades the scale of integration, available materials, batch-production yields, reliability, and raw performance of high-frequency and high-speed components have steadily improved. Thus, many frequency and speed requirements previously met with large volume and weight components are now achievable with miniature lightweight and highly reliable devices. However, cost reduction has recently achieved a plateau indicating that conventional planar technology has reached its limitations and cannot address the needs of the next generation of communication systems and microwave or millimeter-wave radars.



(a) (b)

Fig. 1. Satellite communications. (a) Today's technology. (b) Future technology.



(a) (b)

Fig. 2. Microstrip line. (a) Conventional. (b) Finite ground.

Future communication satellite systems must have minimal spacecraft mass for smaller launch vehicle employment. In addition to reduced size, to maximize returned data and minimize ground operation costs, communication systems are moving up in frequency to Ka-band (25–40 GHz). This will enhance solar-system exploration, global environment understanding, and development of the information superhighway. Furthermore in addition to decreasing spacecraft size, the functionality of the platforms are increasing, necessitating the use of highly integrated sensors and instruments. One area of improvement in reducing size is electronic packaging, which can account for up to 30% of the overall spacecraft mass, and the telecommunication subsystems, which account for 15% or more of the dry mass. Based on this information, advanced high-frequency microelectronics high-density integration (HDI) and on-wafer packaging is a key to reducing volume and mass, while improving performance.

The next leap beyond the current state of the art for the presently used multichip module (MCM) is the development

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TABLE I
50-Ω MICROSTRIP LOSSES AT 30 GHz [5]

Substrate Thickness (μm)	Line Width (μm)	Metal Thickness (μm)	Loss (dB/mm)
2.5 (polyimide)	5	3	0.5
7 (polyimide)	34	3	0.25
500 (hi ρ Si)	420	8	0.05

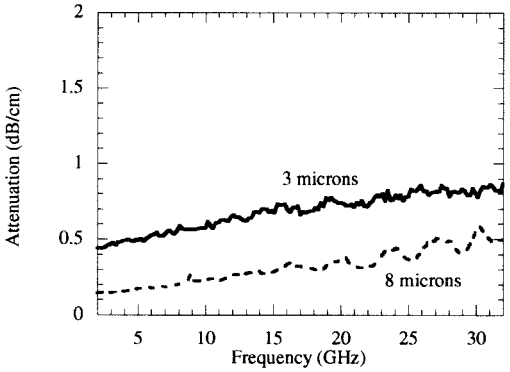


Fig. 3. Measured microstrip line loss versus frequency for two lines of different metallization thickness.

Fig. 4. Alternative microstrip geometries ($h >= 30\ \mu$m).

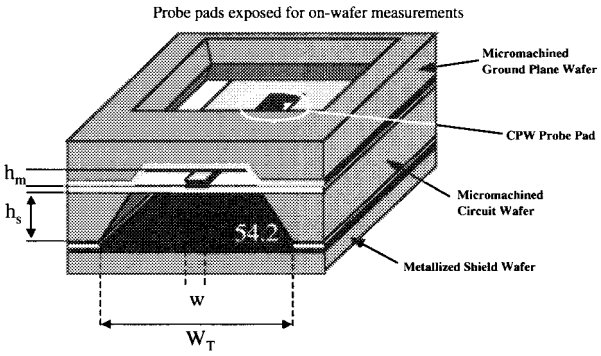


Fig. 5. Membrane microstrip [7].

of a technology which can provide monolithic integration of Si (or SiGe) circuits, advanced microelectromechanical (MEMS) devices, micromachined analog components (e.g., filter/multiplexers), and digital CMOS-based processing circuits into one wafer. Fig. 1 shows both traditional and future front-end communication satellite implementations. The use of electronics in space poses interesting, but grand, challenges. It also provides the opportunity for using revolutionary concepts in circuit design, fabrication, and implementation to achieve what is considered by today's standards as ultimate performance, minimal volume, and very low cost.

Circuit miniaturization can be easily achieved by means of true three-dimensional integration where circuits are laid in all spatial dimensions. This approach has been effectively used in the design of microprocessors and has resulted in a dramatic reduction of size and an unbelievable increase in speed. In combined digital and low-frequency analog applications, multilevel integration results in circuits with multiple power and ground planes and with stripline or microstrip signal lines transitioning between various levels using plated-through vertical interconnects. This integration approach has been proven very effective for clock rates on the order of a few hundred megahertz generating signal harmonics reaching into the low gigahertz range [1]. A similar approach was recently used to provide HDI in high-frequency RF circuits, and provided vital integration solutions for frequencies up to K-band. This HDI approach relies on the use of microstrip technology on very thin (10–20 μm) polyimide layers to provide lines that transition to various planes while sharing the same ground printed at the lowest level of the three-dimensional interconnect structure [2]. The use of a single ground, which does not follow the microstrip lines as they transition into the various planes, in addition to high ohmic loss due to the narrow signal lines (5–34 μm), limits this approach to only a handful of applications and relatively low frequencies of operation.

When conventional lines such as microstrip and coplanar waveguide (CPW) are tested in a three-dimensional environment, their performance typically degrades at higher frequencies due to parasitic radiation and coupling, as well as parasitics from metallized packages or carriers. To avoid these parasitic mechanisms, novel transmission-line designs are required. In this paper, we will review various types of transmission lines on high-resistivity silicon appropriate for RF applications and discuss the beneficial performance trends and circuit architectures as operating frequencies increase to the millimeter-wave regime. Furthermore, we will discuss issues involved with packaging and interconnects for use in three-dimensional vertically integrated circuits.

II. TRANSMISSION LINES FOR VERTICALLY INTEGRATED CIRCUITS

The better the confinement of a wave, the higher its propagation efficiency. This observation has been made repeatedly since the first attempts to use electromagnetic (EM) waves for signal transmission. As in the case of metallic waveguides, two-dimensional confinement may be provided by perfectly shielding the waves using a conducting wall. This perfect confinement forces the field to propagate only after the operation frequency has increased above the natural resonant frequency of the metallic structure (cutoff frequency) and exhibits a frequency-varying phase velocity, a high-frequency

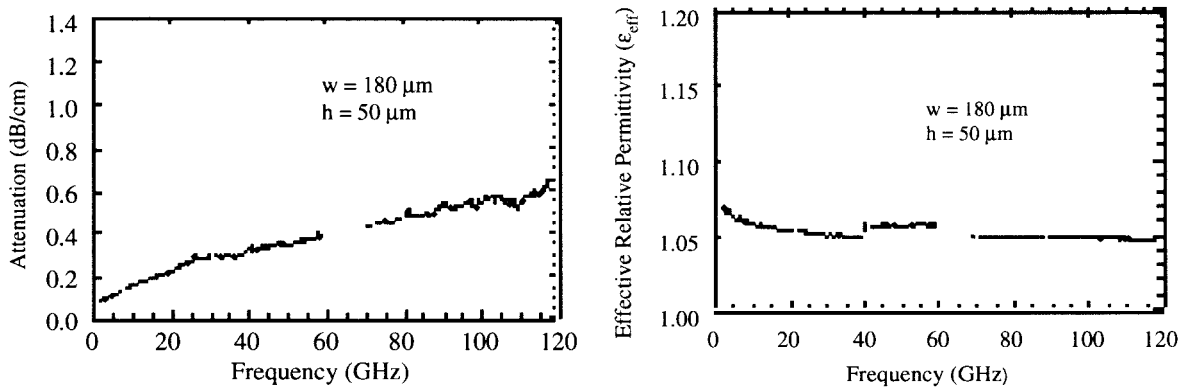


Fig. 6. Measured membrane microstrip loss and effective relative permeability.

effect known as dispersion. To allow for propagation at lower frequencies, avoid dispersion, and eliminate relatively large metallic structures, wave guidance based on field containment rather than field shielding has been developed and used extensively in a variety of applications and frequency ranges. These waveguides, known as transmission lines, are based on the idea of simultaneously using two out-of phase currents to effectively sustain a propagating nonradiating EM wave. Two or more conductors, known as the signal and ground conductor(s), support the two out-of-phase currents, resulting in pure field cancellation everywhere, except between the conductors. The first transmission lines, the coaxial line and the two-wire line, found extensive use in low-frequency systems and demonstrated very effective wave-guidance capabilities in the first communications systems. With the advent of planar technology, transmission lines such as microstrip lines, striplines, coupled strips, and CPW's replaced the coaxial waveguide and the two-wire line. Yet, high propagation efficiency has remained an important factor in circuit design due to the presence of the substrate and its tendency to introduce parasitic mechanisms that impede line performance. Specifically, parasitic junction capacitances result in additional mismatch while wave leakage, in the form of substrate modes, and dielectric loss substantially compromise the power-delivering capability of the transmission line.

There are several reasons for the attenuation of signals traveling through a transmission line. Of those, conductor, dielectric, and radiation losses are the most prevailing form of loss in a planar transmission structure. Conductor losses are caused by the resistive nature of the conductors that force the signal to penetrate through the conductor material. At microwave and millimeter-wave frequencies, current density is maximum at the surface of the conductor and decreases exponentially with depth into the conductor resulting in heat generation and power loss known as ohmic loss. The penetration depth of the current is defined as the skin depth of the line, and is a function of frequency f and the resistivity ρ of the conducting material, as given by the following relationship: $\delta = (1/2\pi)\cdot\sqrt{\rho/f\mu}$. In the case of lossy conductors, it can be shown that signal attenuation measured in decibels/centimeters is inversely proportional to skin depth. As a result, a line of fixed physical length exhibits an ohmic loss that varies

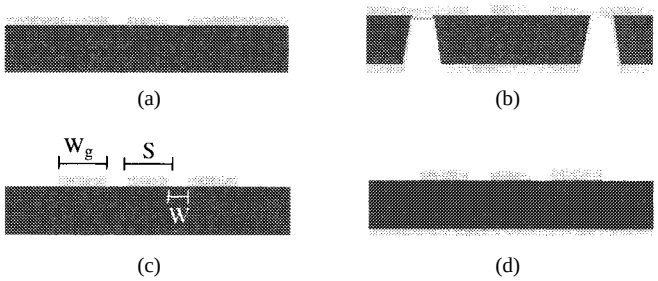
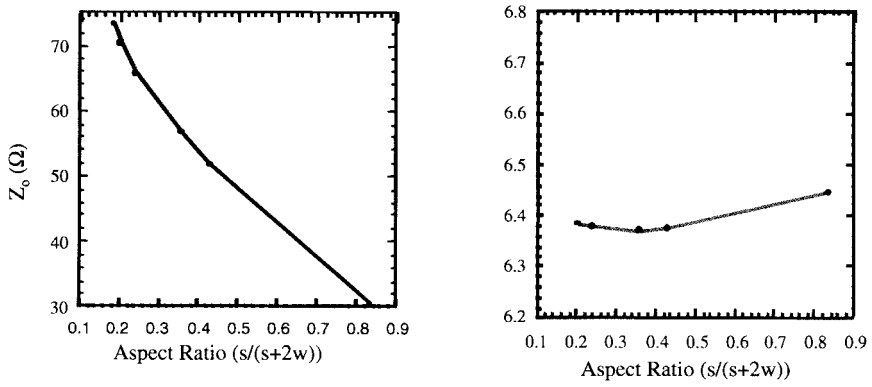


Fig. 7. CPW. (a) Conventional CPW. (b) CPW with backside metallization. (c) FGC. (d) FGC with backside metallization.

with frequency as $\sqrt{f}$. For microwave and millimeter-wave applications where all physical lengths scale with frequency, ohmic loss is measured in decibels per guided wavelength (decibels/λ_g) and exhibits a frequency variation proportional to $1/\sqrt{f}$.

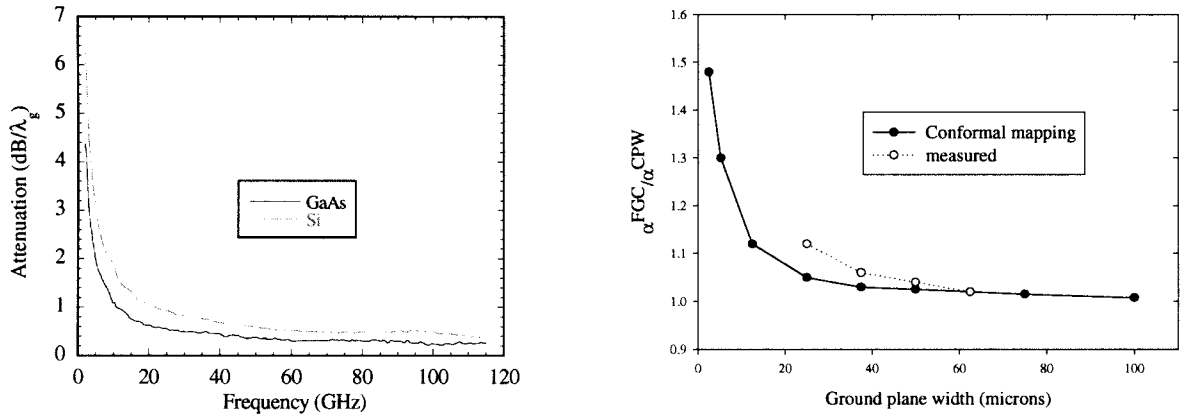
In planar transmission lines, dielectric loss is introduced whenever the excited field is partially or entirely distributed inside a substrate. This is because the medium will absorb part of the transmitted energy due to the presence of polarization charges and their inability to instantaneously follow the changes in the induced electric field. The resulting loss, known as dielectric loss, if measured in dB/λ_g, shows a constant behavior independent of operating frequency. In addition to ohmic and dielectric loss, planar transmission lines operating in an open or semiopen environment suffer from parasitic radiation that may happen either in a distributed way along the length of the line or can be localized at discontinuities. Distributed radiation can be minimized by designing the line to operate in the dominant mode, while localized radiation is more difficult to suppress as it increases with increased discontinuity parasitics.

There are two transmission-line geometries best suited for vertically integrated interconnect networks: microstrip and CPW. Both are popular transmission lines, primarily because they can be fabricated with photolithographic processes and can be easily integrated with other active and passive devices. Each geometry can be modified using micromachining [3] to provide equivalent structures that exhibit much better electrical performance at the cost of higher fabrication complexity. In the following, we will discuss the advantages and disadvantages



(a) (b)

Fig. 8. (a) Characteristic impedance and (b) ε_{eff} for various FGC aspect ratios where s is the center conductor width and w is the aperture width.



(a) (b)

Fig. 9. (a) Attenuation versus frequency for 50-Ω FGC line on Si and GaAs. (b) Attenuation of FGC lines with $S = W = 25$ μm normalized to the attenuation of conventional CPW of the same dimensions versus ground-plane width [9], [10].

of each line, particularly with respect to signal attenuation and line size.

A. Microstrip Line

A microstrip line is a planar waveguiding structure characterized by two conductors facing opposite sides of the dielectric substrate [see Fig. 2(a)]. In all monolithic applications, the utilized microstrip geometry has an infinitely large ground in order to reduce ohmic losses to a minimum. In these circuits, the line characteristics are determined by the substrate thickness, linewidth, and dielectric characteristics of the substrate. While infinite ground minimizes the line loss for a given linewidth, it introduces new problems in packaging and circuit integration. Specifically, it has been extensively observed that lines that share the same ground experience reduced isolation and require wider separations to achieve specific coupling requirements. Also, infinite ground makes vertical line integration difficult. To design lines that can transition vertically into higher or lower planes in a three-dimensional circuit, the ground has to be finite [see Fig. 2(b)] and also transition vertically with the line in a way that preserves field confinement and line characteristics. To leave the microstrip mode uninterrupted, the ground must extend approximately two substrate thicknesses to either side of the microstrip conductor edges $(G = W + 4h)$. However, in many designs, narrower ground conductor widths may be desirable in an effort to achieve higher line impedances. Finite-ground microstrip lines imply higher conductor loss compared to the conventional microstrip, due to the increased line surface resistance at current crowding locations. This is in addition to increased ohmic loss due to electrically narrow center conductors resulting from very thin substrates, such as in the case of the HDI approach [2], [4].

As demonstrated by an extensive study presented in the literature [2], [4], conductor loss in microstrip lines varies inversely with the width of the line and is the dominant component when the substrate thickness becomes electrically small. This is a direct consequence of the frequency variation of each loss component. Table I shows the measured loss of 50-Ω microstrip lines printed on a variety of substrates and operating at 30 GHz. These measured results indicate that lines suffer substantial loss when the linewidth reduces to a few microns. Fig. 3 shows the measured loss in a microstrip line printed on high-resistivity Si substrate for two different metal thicknesses (3 and 8 μm) for frequencies up to 32 GHz and indicate that line loss reduces considerably when the metal thickness increases to many skin depths.

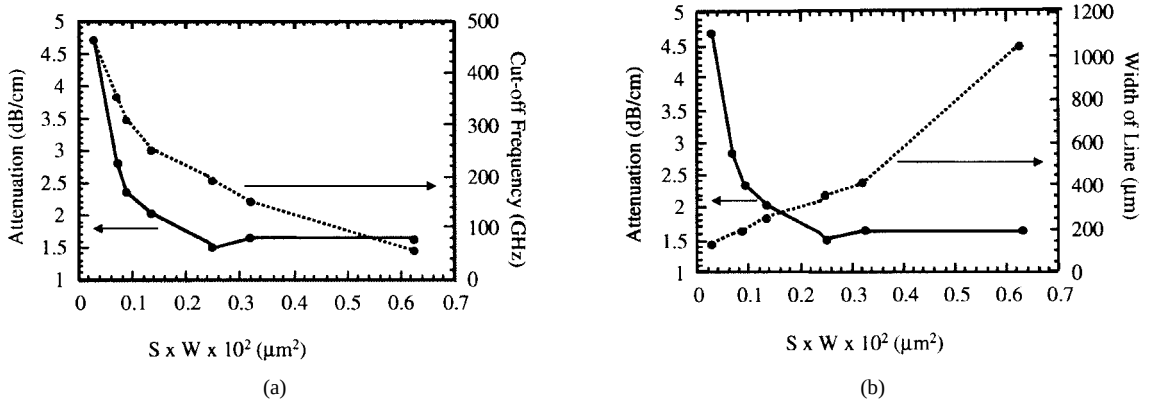


Fig. 10. Attenuation, (a) cutoff frequency, and (b) linewidth versus $S * W$. All measurements performed on silicon substrates of various thicknesses.

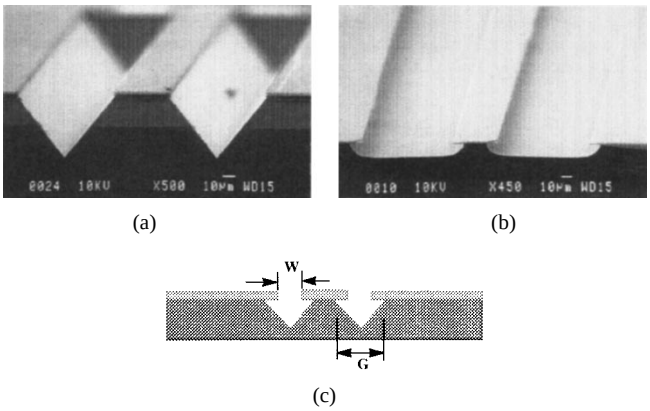


Fig. 11. MFGC waveguide. (a) Anisotropically etched. (b) Isotropically etched. (c) Schematic showing lateral undercut.

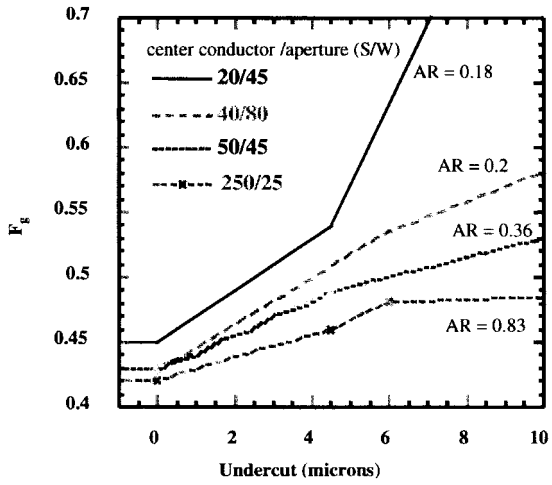


Fig. 12. F_G versus undercut for four different aspect ratios [8].

In microstrip circuits, dielectric and radiation losses may be reduced by decreasing the substrate thickness. As mentioned earlier, the presence of the substrate increases parasitic capacitance and radiation resistance at junctions and transitions, and makes the line susceptible to radiation from these discontinuities. To reduce this radiation, the line capacitance can be increased by locally reducing the substrate thickness, as shown in Fig. 4, where lines have been printed on high-resistivity micromachined Si substrates. In Fig. 4(a), the substrate has been removed underneath the line using anisotropic wet etching [potassium hydroxide (KOH) or ethylenediamene pyracatechol (EDP)] [3] to reduce the effective dielectric constant and improve TEM propagation. In Fig. 4(b), the substrate has been removed and the etched cavity has been metallized to improve propagation efficiency. In addition to fabrication difficulties, thinner Si or GaAs substrates for the arrangement of Fig. 4(b) are not recommended due to the narrow linewidths required and the subsequent increase in conductor loss.

B. Membrane Microstrip

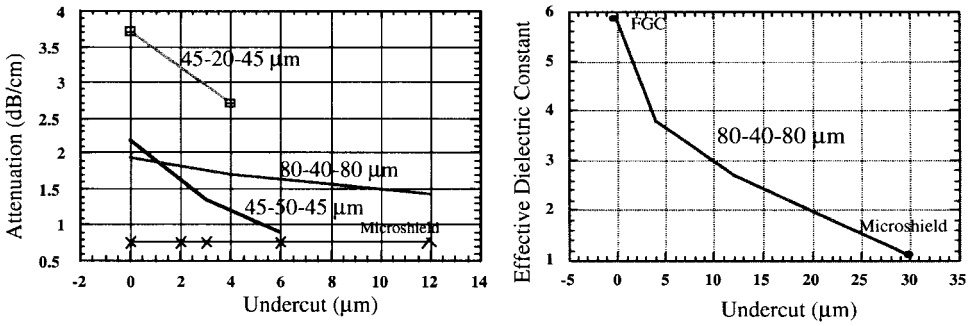
To reduce dielectric loss and parasitic capacitance, and increase line impedance, a micromachined version of the microstrip has been developed (see Fig. 5) and extensively used in high-frequency applications including Ka-, V-, and W-band filters and broad-band couplers [5], [6]. Due to the fact that the substrate material has been removed, the exhibited loss is only of conductor type and is considerably lower than any other microstrip line due to the higher line characteristic impedance. The total width of this line W_T is given by the following equation [7]:

$$W_T = 5h_m + 2h_s \tan(57.2^\circ) \tag{1}$$

where h_m is the distance of the microstrip from the ground plane and h_s is the lower substrate thickness, as shown in the figure. In (1), 57.2° is the angle of the sidewalls produced by the wet etchant as it etches selectively along the $\langle 111 \rangle$ silicon crystal planes. The loss of this line has been measured up to W-band and has been found to be the lowest exhibited by a planar line in that frequency range. This loss is equal to approximately 0.5 dB/cm at 94 GHz, which is approximately twice as high as the loss exhibited by a metallic waveguide operating in the same frequency range. Loss measurements and the effective dielectric constant for this line are shown in Fig. 6.

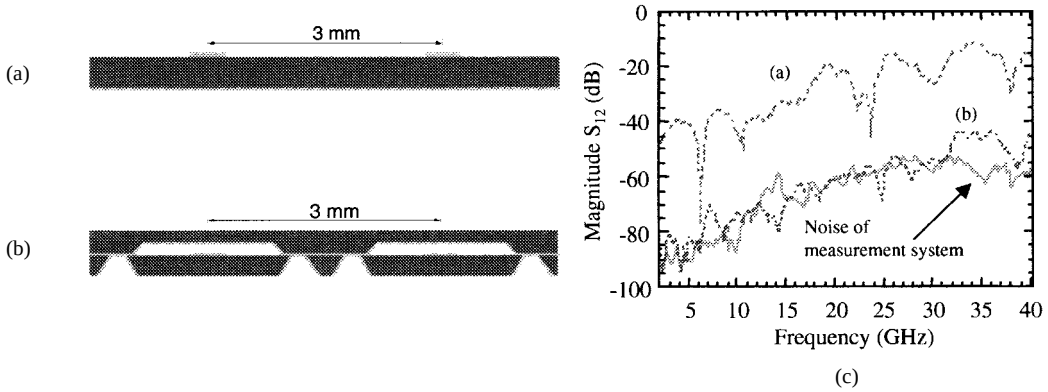
C. Finite Ground CPW

Compared to other types of coplanar lines, shown in Fig. 7(a) and (b), finite ground coplanar (FGC) waveguide [see Fig. 7(c) and (d)] is a uniplanar line that exhibits excellent characteristics. The geometrical parameters important in



(a) (b)

Fig. 13. (a) Attenuation and (b) effective dielectric constant versus frequency for MFGC lines at 94 GHz.



(c)

Fig. 14. Packaged microstrip line. Cross coupling of adjacent circuits. (a) Conventional (unshielded) microstrip. (b) Completely shielded microstrip (c) Measured cross coupling [12].

determining characteristic impedance, dielectric constant, and losses are the ground conductor width W_g, aperture width W, center conductor width S, and effective dielectric constant ε_{eff}. Design curves derived by use of a combination of static analysis and conformal mapping [8], [9] for the lines characteristic impedance and dielectric constant are shown in Fig. 8 as a function of the aspect ratio $[AR = (S/(S+2W)]$.

The major advantage of the FGC line [see Fig. 7(c)] is its ability to suppress parasitic parallel-plate modes. As a result, it does not require vias for ground equalization, and its propagation characteristics are not sensitive to the substrate thickness and presence of backside metallization [see Fig. 7(d)]. The line geometry allows for control over the cutoff frequency of the higher order modes through the relation

$$(2W_g + 2W) + S \leq \lambda_g/2. \tag{2}$$

When the line is designed so that it operates in the CPW mode regime, the line attenuation is only attributed to conductor loss. Extensive measurements performed between 10 and 110 GHz show a loss factor which in decibels/λ_g varies as function of $1/\sqrt{f}$, as shown in Fig. 9(a) [10], and is practically independent of the substrate. When the width of the ground plane becomes smaller, the loss factor starts increasing and becomes noticeable when the ground conductor width becomes less than 1.5 times the width of the center conductor. Fig. 9(b) shows theoretical and experimental results for the loss of the FGC line for various ground-plane widths [9].

The loss of the FGC line varies inversely with the product of the aperture width and the separation. As a result, lower losses require larger linewidths and lower cutoff frequencies. Fig. 10 shows data from measurements performed on lines of different characteristic impedances using thru-reflection line (TRL) calibration [8], [9]. These data clearly indicate a monotonic decrease of the loss with increasing product $S*W$. This curve by itself is not very helpful in design unless the dependency of the size of the line or of the cutoff frequency for the same product is known. The two plots in Fig. 10 show loss, linewidth, and cutoff frequency variation versus $S*W$. These trends hold true for lines printed on different substrates, having different S and W, but the same $S*W$ product.

D. Micromachined FGC (MFGC) Waveguide

Since the FGC waveguide exhibits only conductor loss, the only electrical parameter that can influence the loss factor is the characteristic impedance. Higher Z_o reduces the electric-current distribution on the conductors and results in lower conductor loss. There are two design methods that may directly reduce conductor loss by increasing the characteristic impedance: varying the aspect ratio $[AR = S/(S+2W)]$ and removing dielectric material from the aperture regions. In the former approach, higher characteristic impedances are realized by wider aperture width W or wider total width $[S+2(W+W_g)]$. As a result, higher line impedance requires larger line dimensions, and lead into lower cutoff frequencies and a limited single-mode frequency range. To avoid reducing

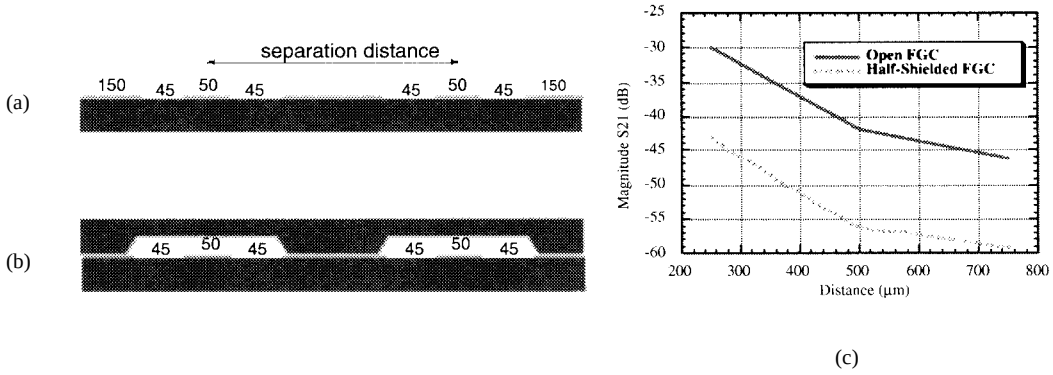


Fig. 15. (a) Conventional GFC. (b) Packaged FGC line. (c) Computed coupling between open and half-shielded 45–50–45-μm FGC lines with shared grounds for 10 GHz [20].

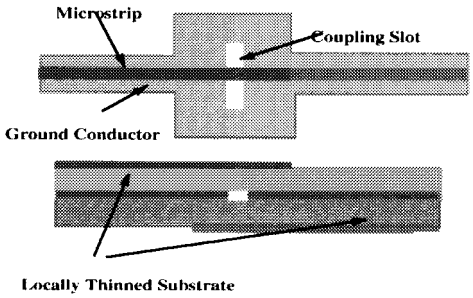


Fig. 16. Microstrip vertical transition.

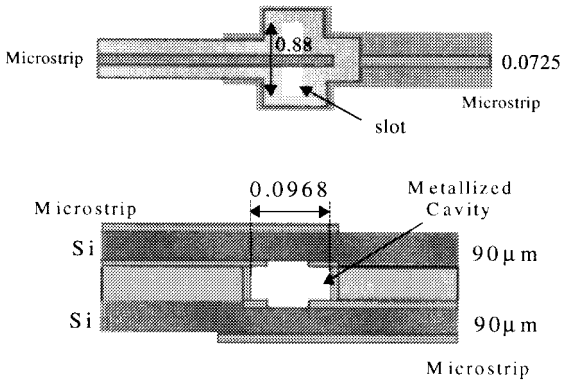


Fig. 17. Multilayer microstrip transition. All dimensions in microns.

the effective bandwidth of the line, material can be removed from the area underneath the apertures of the line resulting in reduced effective dielectric constant, lower line capacitance, higher characteristic impedance, and lower ohmic loss [8].

The material underneath the line may be removed with a variety of techniques, including wet etching or reactive ion etching. Wet etching results in a pyramidal or cylindrical groove depending on the type of etchant, e.g., KOH, EDP, or tetramethyl ammonium hydroxide (TMAH) give an anisotropic profile while HF/Nitric yields an isotropic one (see Fig. 11). The larger the width of the groove, the greater the material removed. Substantial changes of the line characteristics are observed as the groove width G approaches and exceeds the aperture width W. Let us define the undercut U of the line as $U = (G - W)/2$. From all the geometrical parameters characterizing the groove size, the undercut U will be used herein to quantify the groove effects on line performance. MFGC lines exhibit lower effective dielectric constants due to the presence of air regions underneath the apertures [8]. Fig. 12 shows F_G defined by $F_G = (1/\sqrt{\varepsilon_{\text{eff}}})$ as a function of the undercut U for four different aspect ratios. For the line with aspect ratio 0.18 as noted on the figure, F_G has a value close to 0.45 when no material is removed, and increases to 0.7 when 7 μm of undercut is achieved. In the limit for any line when all material is removed, F_G will approach one. Note that lines with wider apertures W and narrower center conductors S tend to converge to one faster. These micromachined lines have higher cutoff frequencies than the regular FGC of the same aspect ratio. Specifically, the ground conductor width of the line can be specified so that the cutoff frequency of the higher order mode is above the higher frequency of interest $2(W_g + S) + W \leq F(\lambda_o/G_2)$, where λ_o is the free-space wavelength of the highest cutoff frequency.

The loss of the line decreases monotonically with the undercut U, as shown in Fig. 13, and reduces well below the values characterizing the FGC line of the same aspect ratio. The loss of the MFGC lines approaches the loss of a microshield line (CPW suspended on a membrane [11]), as shown in the same figure. This comparison indicates that the MFGC is the lowest in loss after the microshield line and the second lowest after the metallic waveguide.

III. On-Wafer Packaging of Lines for Vertical Integration and EM Coupling

When microstrip and coplanar lines are printed in high-density configurations, minimizing interactions between adjacent circuits becomes extremely important. This interaction, known as crosstalk, may be due to substrate modes or parasitic coupling capacitances and results in degraded electrical performance. In high-density circuits, on-wafer packaging becomes an important means of isolating circuits while preserving the integrity of performance and the monolithic character of the circuit. With multilayered configurations, the vertical stacking of substrates necessitates packaging and requires different designs intended for microstrip or CPW circuits with the requirement that all conductors be of finite size. On-wafer packaging of a microstrip is more difficult to perform than that of coplanar structures simply due to the possible distances that can be achieved between the line conductors.

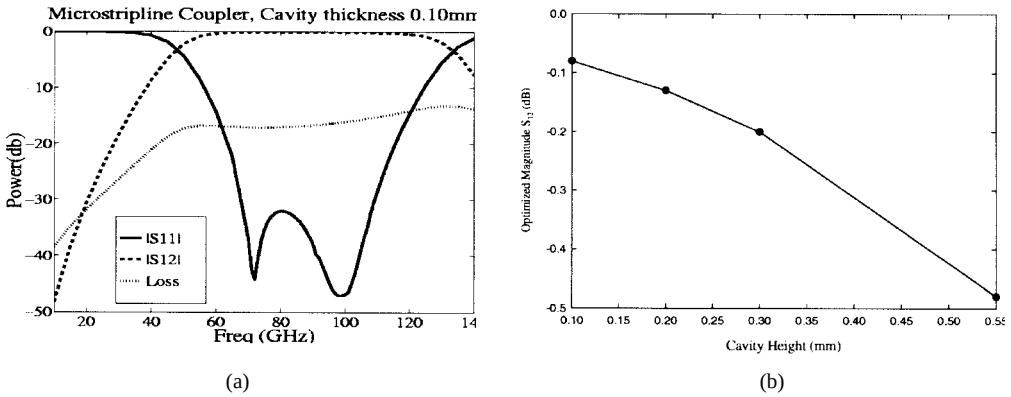


Fig. 18. (a) Computed results through W-band for microstrip coupler of Fig. 17 with cavity 0.1 mm in height. (b) Optimized insertion loss versus cavity height.

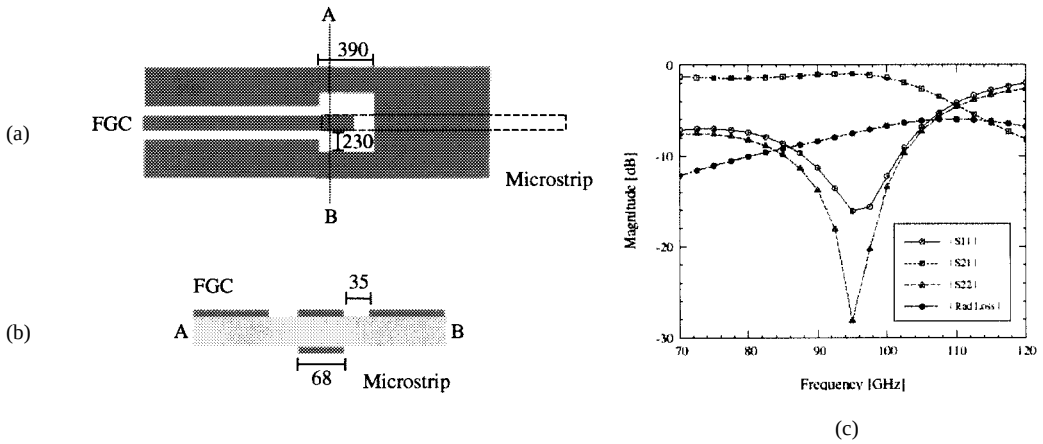


Fig. 19. FGC-to-microstrip transition on 100-μm-thick silicon. All dimensions shown in micrometers. (a) Schematic. (b) Cross section AB. (c) S-parameters.

In microstrip, the distance between the two conductors is determined by the substrate thickness, but in the CPW the same distance is determined by the circuit designer based on loss or line impedance requirements. To ensure package noninvasiveness, it is important to minimize the distance between the line conductors (slot apertures) and improve field confinement.

If the packaging cavity is to provide EM shielding in addition to physical protection, cavity surfaces must be coated with a conductive layer. In order to keep the potential of the conducting layer of the package from floating away from that of the ground conductor, resulting in additional parasitic capacitances, the ground conductors of the package should be brought to the same potential with the microstrip ground. This requires the shielding configuration, shown in Fig. 14(b), in which the conducting surfaces of the cavity and the microstrip ground meet each other halfway at same level with, but on either side of, the center conductor. For high isolation requirements, silicon micromachining of the circuit can provide on-wafer packaging of a microstrip circuit that reduces EM coupling between adjacent lines to significantly low levels. Fig. 14(c) shows substantial improvement in electrical performance demonstrated by a conformally packaged microstrip line compared to an unpackaged conventional one. Lower loss versions of the line may be made by thinning the middle portion of the lower substrate or removing it completely, as done for the membrane microstrip line. However, when these packaging options are considered, circuit structural integrity becomes an issue.

Packaging for FGC lines is easier because the ground planes and center conductor are on the same planar surface. As a result, ground equalization is achieved along the sides of the package where it interfaces with the FGC ground planes [see Fig. 15(b)]. Packaging in FGC is important for the following three reasons:

1) to create an air region above the apertures and keep dielectric loss minimized;
2) to provide a cavity for air-bridge protection;
3) to provide EM shielding and further reduce coupling.

Adjacent FGC lines naturally have high isolation due to very good confinement in the aperture regions. As an illustration of this, coupling measurements between two open 50-Ω FGC lines (45–50–45 μm) with 150-μm-wide grounds, as shown in Fig. 15(c). These results indicate that lines as close as 250 μm (center-to-center) couple less than -30 dB [10]. However, the upper shielding of the FGC can further reduce coupling, as shown in Fig. 15(c), which presents computed values of the coupling between adjacent lines. Coupling below -45 dB for separations as close as 250 mm is demonstrated. Note in these full-wave calculations performed by HFSS[1] that the lines share the same ground plane. When adjacent lines do not share the same ground planes, isolation better than -50

[1] HFSS, Ansoft Version 1.9.04, Ansoft Corporation, Pittsburgh, PA.

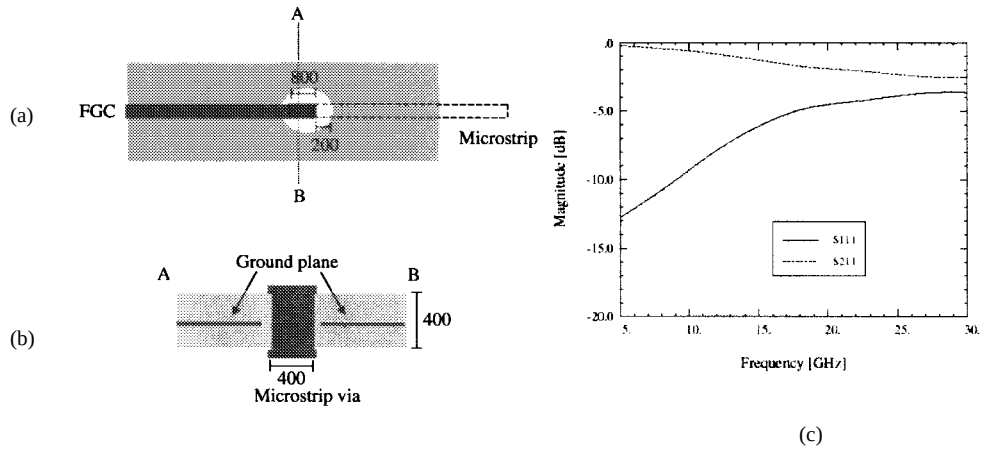


Fig. 20. Microstrip-to-microstrip transition on 400-μm-high Teflon ($\varepsilon_r = 4.5$). Center conductor width = 400 μm, via is 800 μm on each side. (a) Schematic. (b) Cross section AB. (c) Theoretically calculated S-parameters using FEM.

dB can be easily achieved. The lower loss MFGC lines may be simply packaged in the same method as the conventional FGC line.

IV. Vertical Transitions

Both microstrip and FGC waveguide lines have been considered for use in vertically integrated circuits. These three-dimensional circuits require multiple transitions between layers including signal transmission from one side of a wafer to the facing side of an adjacent wafer, through one silicon layer, and/or through two or more layers. In high-frequency applications, in contrast to digital circuits, vertical transitions have to be particularly designed to provide very low return loss, wide bandwidth, and very high transmission efficiency. Designs that provide very low transition parasitics, ohmic loss, and radiation are investigated and the results from this study are presented here. There are two design approaches that are followed in the development of high-frequency vertical transitions: EM coupling and direct contact. Results from the application of these two approaches will be discussed in detail below.

A. Electromagnetically Coupled Transitions

1) Microstrip-to-Microstrip Transitions: Two-layer microstrip transitions in W-band may best be performed through a coupling slot printed on the microstrip ground, as shown in Fig. 16. These transitions have been utilized extensively and can provide less than 0.5-dB insertion loss and very broad bandwidths. The length of the slot required for a transition is between one-fourth and one-third of the microstrip guide wavelength, thus allowing the slot to parasitically radiate with the appropriate phasing. In this manner, the radiated field effectively couples back to the two microstrips and provides an excellent transition. When the slot orientation with respect to the two lines is altered, the transition suffers from considerable radiation loss from the coupling slot. Extensive experiments on X- and K-band transitions have confirmed the theoretical data and demonstrated excellent performance [13], [14].

Transitions through multiple layers require a more complex structure, such as the one shown in Fig. 17. In this arrangement, the ground of the two microstrips is connected

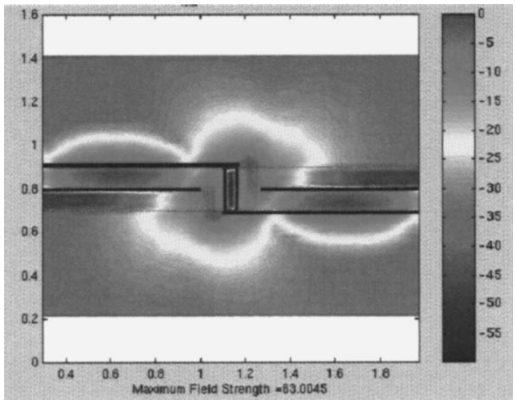


Fig. 21. Total electric-field plot of microstrip-to-microstrip transition at 95 GHz based on theoretically obtained FEM results.

through a short section of a narrow waveguide which carries the EM power from one side of the transition to the other. Theoretically calculated insertion loss for this transition is shown in Fig. 18(a) as a function of frequency for 50-Ω microstrip input and output lines printed on 100-μm high-resistivity Si layers. These data have been completed by a hybrid finite-element method/method of moments (FEM/MoM) and assume perfect conductors and lossless dielectrics. Only radiation loss is included in this modeling [20]. Additional calculations indicate that insertion loss increases to 0.5 dB as the cavity thickness increases from 100 to 500 μm and beyond [see Fig. 18(b)]. Furthermore, studies performed have indicated that the performance of the transition is insensitive to misalignment on the order of 10–20 μm. Although these designs have not yet been fabricated, it is expected that measurements will only add approximately 0.1–0.2 dB of extra loss due to finite conductivity in the evaporated metals.

2) Microstrip to CPW Transitions: Fig. 19 shows an electomagnetically coupled microstrip-to-CPW transition on 100-μm-thick high-resistivity silicon. Numerical simulations from IE3D[2] show insertion loss of -1 dB and return loss below -15 dB at 95 GHz. The radiation loss at this frequency is close to -8 dB. The same transition designed for X- or K-

[2] IE3D, Release 4, Zeland+ Software, Inc., Fremont, CA, 1997.

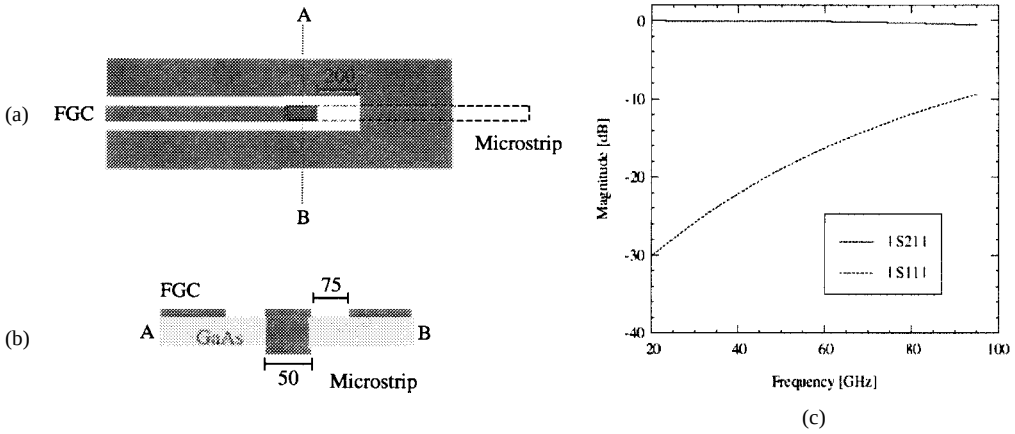


Fig. 22. CPW-to-microstrip transition designed on 100-μm-thick GaAs ($\varepsilon_r = 12.9$) with via dimensions 50 μm $\times$ 75 μm. All other dimensions in microns. (a) Schematic (b) Cross section AB. (c) Theoretically calculated S-parameters using FEM.

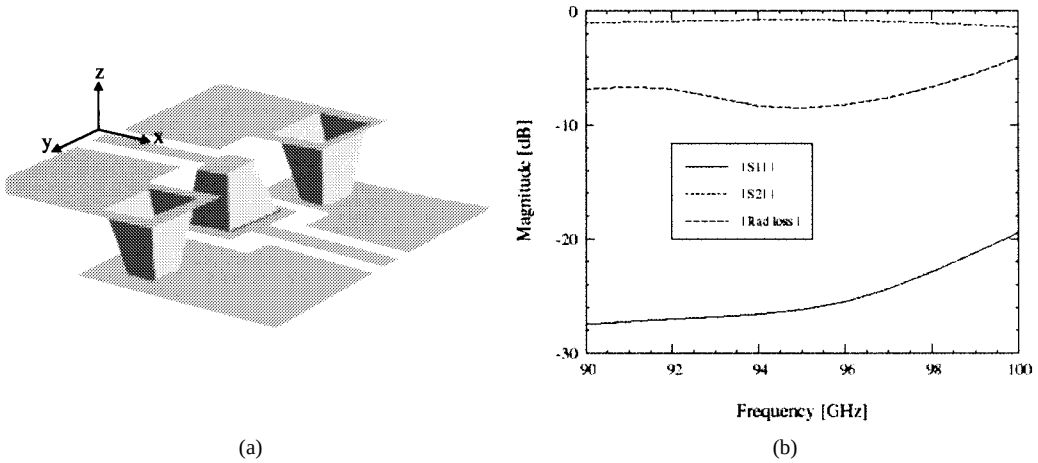


Fig. 23. CPW-to-CPW transition. (a) Schematic. (b) S-parameters, including radiation loss (FEM).

band application will result in much better performance due to electrically reduced substrate thickness and better coupling between the two lines. In this transition, as with the previous one, theoretical results have been derived assuming perfect conductor and lossless dielectrics.

B. Direct-Contact Transitions

1) Microstrip-to-Microstrip Transition: Microstrip transitions involving direct contact must contend with the ground-plane issue. One design is shown in Fig. 20(a) and (b), in which the ground plane is shared by both conductor lines and is interrupted by a circular aperture etched around the via connecting the two microstrip lines. This transition is characterized by increasingly poor performance as frequency increases. Numerical simulations using the FEM performed on a shielded transition made of lossless metal printed on two 400-μm-thick lossless Teflon layers have shown drastic degradation of the input return due to the parasitic inductance of the via. Fig. 20(c) shows theoretical insertion loss of -0.3 dB and return loss of -13 dB at 5 GHz. The same transition when operating in an open environment exhibits increasing radiation due to the increased electrical length of the via at higher operating frequencies. The total electric field

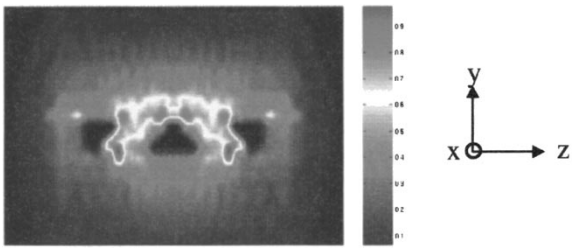
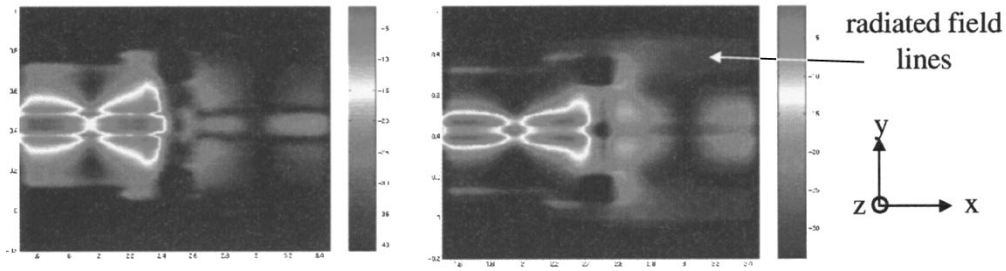


Fig. 24. Electric-field distribution for yz-plane of Fig. 23.

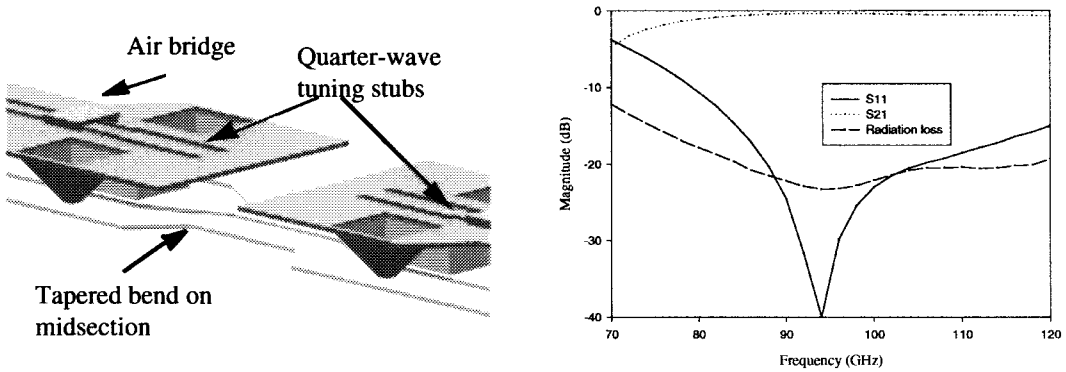
excited around the via when operating in an open cavity is shown in Fig. 21, and indicates high radiation by the extensive spread of the field lines. This design may be optimized for operation at higher frequencies by choosing thinner substrates.

2) CPW-to-Microstrip Transition: A CPW-to-microstrip transition has been examined in which a single via connects the center conductor of the CPW line to the strip conductor of the microstrip while the ground planes are shared (see Fig. 22). Simulated results with FEM for a shielded line demonstrate improved performance in this design, as opposed to the microstrip-to-microstrip design, with insertion loss of -0.01 and return loss of -30 dB at 20 GHz. Performance degrades at higher frequencies due to the parasitic inductance.



(a) (b)

Fig. 25. Electric-field distribution for xy-plane of Fig. 23. (a) z-component of the electric field vector for the transition of Fig. 23. (b) Total electric-field distribution for the transition of Fig. 23 showing launched horizontal electric-field component.



(a) (b)

Fig. 26. (a) An FGC vertical interconnect employing three micromachined pyramidal via holes. The vias permeate the Si substrate to connect the upper and lower lines. (Substrate not shown). (b) Theoretically calculated S-parameters of singe transition using IE3D.

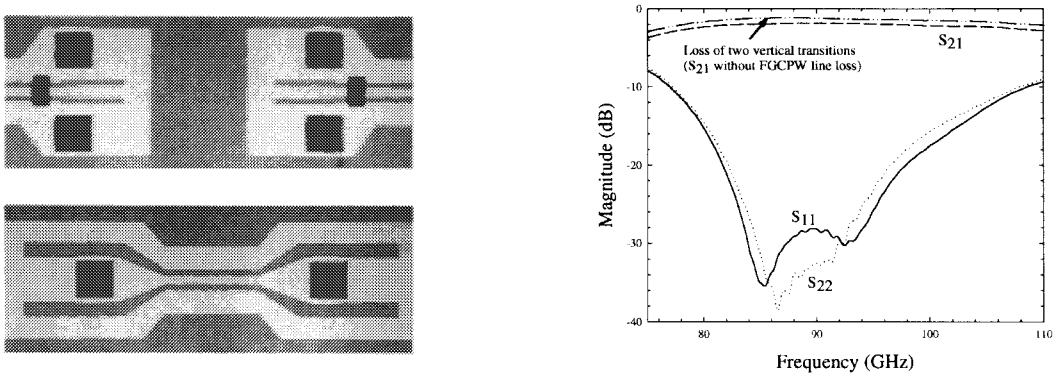
The theoretical values include no ohmic losses, which are expected to reach 0.1 dB at 40 GHz.

3) CPW-to-CPW Transition: Silicon micromachining has been applied to many microwave and millimeter-wave circuits, and has offered new methods of vertical integration. To this effect, a micromachined three-via interconnect has been developed and fabricated for CPW-based circuits, providing signal transfer through a silicon wafer. Fig. 23(b) shows calculated insertion loss versus frequency for the transition on a 90-μm-high resistivity substrate with 50-Ω impedance FGC lines that are designed to exhibit a higher order mode above 180 GHz. All conductors and dielectrics are considered lossless. The minimum reflection and insertion loss achieved in this case are -28 and -0.8 dB, respectively, at 90 GHz. As shown in the figure, pyramidal shaped vias completely embedded in the dielectric with 150 μm^2 apertures require wider center conductor and aperture spacing, resulting in a lower line impedance in the via region that needs to effectively transition to the input. By observing the computed values, we can conclude that the insertion loss is mostly attributed to radiation loss which varies from -7 dB at 80 GHz to -3 dB at 100 GHz.

The field in the vias is well confined, as shown in Fig. 24, and does not contribute to the radiation loss. The radiation loss exhibited by this transition is due to the electric field excited at the wider CPW sections connecting the feedline to the via [see Fig. 23(a)]. This field launches a horizontally polarized substrate mode at the terminating edge of the input line, as shown in Fig. 25. The field along the input and output lines is well confined, as shown by the well-defined standing waves that are also shown in Fig. 25. The calculations of these field distributions have been performed by the FEM and have considered that the feedlines are terminated at open circuits and are excited by ideal current sources, which is why the fields on the two lines exhibit strong standing waves.

To resolve the radiation problem, the transition from the feed FGC line to the vertical via structure has been modified, as shown in Fig. 26. The two finite grounds have been connected at the end of the line to short circuit any undesired horizontally polarized substrate modes that would tend to launch a parasitic wave from the end of the line. The presence of the short requires a quarter-wave CPW stub to provide an RF open to fields which would tend to propagate horizontally pass the via structure. Furthermore, to cancel the inductive behavior of the via and improve the return loss, a capacitive bridge has been entered right before the via structure as shown [15]. This transition in a back- to-back configuration has been solved numerically using IE3D[2] showing excellent performance with an insertion loss of less than -15 dB from 85 to 110 GHz and radiation loss less than 0.2 dB per transition. These calculations did not include any ohmic or dielectric losses.

Measured results are shown in Fig. 27 for a back-to-back FGC three-via transition, with 1.82-dB insertion loss and 30-dB return loss at 90 GHz. After accounting for the loss of the FGC feeding lines, the loss due to each transition is approximately 0.6 dB, from which 0.2 dB is attributed to radiation losses and 0.4 dB to ohmic losses. Considering that



(a) (b)

Fig. 27. (a) Photo of fabricated back-to-back transition showing feed lines and midsection. (b) Measured S-parameters of back-to-back vertical interconnect transition at W-band.

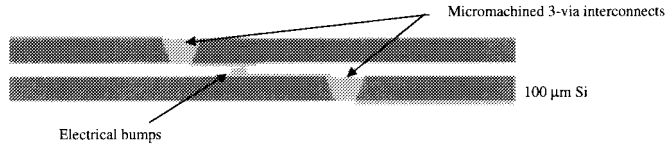


Fig. 28. Possible multilayer configuration.

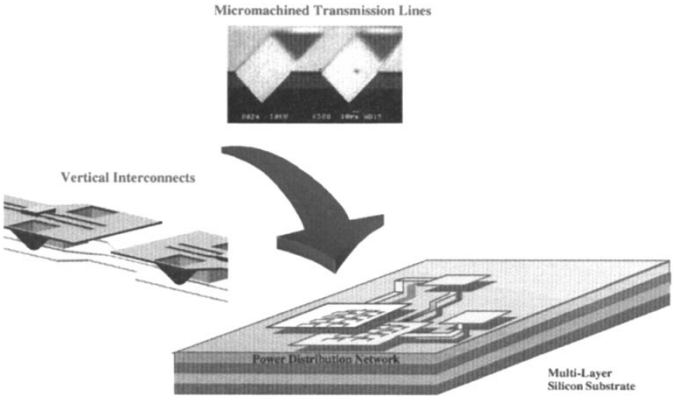


Fig. 29. Integration of micromachined transmission lines and vertical interconnects in a multilayer silicon substrate.

radiation losses scale directly with the operating frequency and that ohmic loss reduces as $\sqrt{f}$, the same transition designed for 30-GHz operating frequency, by changing the length of the short-circuit stub and the size of the capacitive bridge, would exhibit an insertion loss of less than 0.2 dB.

4) Multilayer FGC Waveguide Transitions: Similar to the single-layer transition, a multilayered transition may be performed by cascading multiple transitions. To achieve such a cascade, direct contact transition from one side of a wafer to the facing side of the adjacent wafer needs to be included. This may be done with an extended section of FGC line electroplated to a specified height above the rest of the circuit metal to form three gold bumps. When this is done on facing sides of two silicon wafers, contact may be made using thermal compression. These bump transitions are presently under development, but preliminary results show their potential to provide less that 0.2-dB loss per transition in the form of ohmic loss in W-band. Fig. 28 shows a possible multilayer configuration utilizing micromachined three-via interconnects and soft gold electrical bumps between the two silicon layers.

V. Conclusion

Novel planar transmission lines and vertical interconnects for high-density vertically integrated MMIC circuits have been presented. Depending on the application, both microstrip and FGC waveguide may be appropriate in highly dense circuit areas. For extremely small wafer real estate, microstrip can provide the most compact geometry and may be best vertically integrated with EM-coupled slots and simple fabrication. The proposed micromachined version of the interconnect lines has been made possible by the use of high-resistivity silicon and has demonstrated excellent results. FGC waveguide provides better field confinement and little or no dependence on substrate thickness, making it well-suited for three-dimensional circuits. The direct contact transition utilizing three pyramidal-shaped vias, although more complicated to fabricate, is quite compact both vertically and laterally, yielding loss of 0.6-dB transition at 94 GHz. Additionally, its micromachined version has shown substantial loss reduction with minimal silicon removal in the aperture regions. All the vertical interconnects have been fabricated on high-resistivity Si and have demonstrated excellent performance at frequencies up to 110 GHz. The use of Si has allowed for the development of a variety of micromachined shapes that may provide lower parasitics and better performance. As illustrated in Fig. 29, the developed interconnect and vertical transition schemes have the potential to revolutionize the microwave field by offering new means for interconnecting and integrating high-density high-performance three-dimensional circuits.

References

[1] J.-G. Yook, L. P. B. Katehi, K. A. Sakallah, R. S. Martin, L. Huang, and T. A. Schreyer, "Application of system-level EM modeling to high-speed digital IC packages and PCB's," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1847–1856, Oct. 1997.

[2] P. D. Cooper, P. A. Piacente, and R. J. Street, "Multichip-on-flex plastic encapsulated MHDI-low cost substrates manufacturing for microwave and millimeter wave modules," in *IEEE Microwave Theory Tech. Symp. Dig.*, San Francisco, CA, June 17–21, 1996, pp. 219–222.

[3] L. P. B. Katehi *et al.*, "Si micromachining in high-frequency applications," in *CRC Handbook on Si Micromachining*. Boca Raton, FL: CRC Press, 1995.
[4] G. E. Ponchak, and A. N. Downey, "Characterization of thin film microstrip lines on polyimide," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 21, pp. 171–176, May 1998.
[5] S. V. Robertson, L. P. B. Katehi, G. M. Rebeiz, "Micromachined W-band filters," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 598–606, Apr. 1996.
[6] C.-Y. Chi and G. M. Rebeiz, "Planar microwave and millimeter-wave lumped elements and coupled-line filters using micromachining techniques," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 730–738, Apr. 1995.
[7] S. V. Robertson, "Micromachined W-band circuits," Ph.D. dissertation, Dept. Elect. Eng. Computer Sci., Univ. Michigan at Ann Arbor, 1997.
[8] K. J. Herrick, T. A. Schwarz, and L. P. B. Katehi, "Si-micromachined coplanar waveguides for use in high-frequency circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 762–769, June 1998.
[9] G. E. Ponchak and L. P. B. Katehi, "Finite ground coplanar (FGC) waveguide: A better transmission line for microwave circuits," *Advancing Microelectron.*, vol. 25, pp. 15–18, May/June 1998.
[10] F. Brauchler, "Finite ground coplanar passive and active devices," Ph.D. dissertation, Dept. Elect. Eng. Computer Sci., The Univ. Michigan at Ann Arbor, 1996.
[11] T. M. Weller, G. M Rebeiz, and L. P. B. Katehi, "Experimental results on microshield transmission line circuits," in *IEEE Microwave Theory Tech. Symp. Digest*, Albuquerque, NM, 1993, pp. 827–830.
[12] R. M. Henderson and L. P. B. Katehi, "Silicon-based micromachined packages for discrete components," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Denver, CO, June 1997, pp. 521–524.
[13] N. L. Van den Berg and L. P. B. Katehi, "Broad-band vertical interconnects using slot-coupled shielded microstrip lines," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 81–88, Jan. 1992.
[14] N. L. Van den Berg, "Full wave analysis of microstrip slot antennas and couplers," Ph.D. dissertation, Dept. Elect. Eng. Computer Sci., The Univ. Michigan at Ann Arbor, 1991.
[15] K. J. Herrick, J-G Yook, S. V. Robertson, G. M. Rebeiz, and L. P. B. Katehi, "W-band micromachined vertical interconnection for three-dimensional microwave IC's," in *28th European Microwave Conf.*, Amsterdam, The Netherlands, 1998.
[16] M. I. Herman, K. A. Lee, E. A. Kolawa, L. E. Lowry and A. N. Tulintseff, "Novel techniques for millimeter-wave packages," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 1516–1523, July 1995.
[17] L. P. B. Katehi, "Novel transmission lines for the submillimeter-wave region," *Proc. IEEE*, vol. 80, pp. 1771–1787, Nov. 1992.
[18] G. P. Gauthier, L. P. Katehi, and G. M. Rebeiz, "W-band finite ground coplanar waveguide (FGCPW) to microstrip line transition," in *IEEE Microwave Theory Tech. Symp. Dig.*, Baltimore, MD, June 1998.
[19] R. F. Drayton, R. M. Henderson, and L. P. B. Katehi, "Monolithic packaging concepts for high isolation in circuits and antennas," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 900–906, July 1998.
[20] J.-C. Cheng, "Theoretical modeling of MMIC's using wavelets, parallel computing and a hybrid MOM/FEM technique," Ph.D. dissertation, The Univ. Michigan at Ann Arbor, 1998.
[21] S. Maeda, T. Kashiwa, and I. Fukai, "Full wave analysis of propagation characteristics of a through hole using finite-difference time-domain method," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 2154–2159, Dec. 1991.

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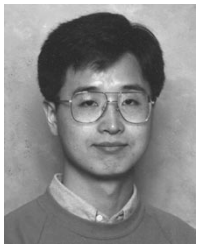

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